



# Study of FinFET based Circuit for Ultra-Low Power Operation

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## ABSTRACT

This work aims at analysing leakage power and its variability of CMOS and FinFET inverter chain at 32-nm technology node. This paper also analyses other design metrics like propagation delay, power-delay product (PDP) and energy-delay product (EDP) of CMOS based inverter and FinFET based inverter. FinFET based inverter design achieves  $1.58 \times (1.32 \times)$ ,  $10.03 \times$ ,  $4.71 \times 5.11 \times$  improvement in leakage power (its variability), propagation delay, PDP and EDP respectively compared to its CMOS based inverter. In this analysis the FinFET based inverter is found to be suitable for ultra-low power applications like portable and wearable devices.

## Keywords

Leakage Power, variability; power-delay product (PDP); energy-delay product (EDP); ultralow-power design.

## 1. INTRODUCTION

Since the advent of semiconductors and throughout the history of designing ICs for everything from computer hardware to mobile phones, the basic principle of Moore's law has persisted to be the same: the number of transistors on a given area of silicon doubles every two years [1]-[3]. The transistor count on today's advanced multicore processors is reaching the range of three billions, a long way from the 6800 processor of the mid 1970s which consisted of just 5000 transistors [4]. Semiconductor manufacturing industries are assisting to the maximum extent to make this growth attainable by introducing scaled CMOS devices using field effect transistor (FET) technology. As the approach is driving towards sub nano meter range that is beyond 90-nm node, leakage became an important factor [5] [6].

While the MOS devices reached the end of its scalable limit, the semiconductor industry found an alternative device such as FinFET, which is considered to be the best choice for next generation devices. Many semiconductor industries are putting their efforts in FinFET technology which helps to continue Moore's law [7]. FinFETs have higher performance and reduced power consumption compared to MOS devices. Silicon film (body) in FinFET is usually undoped or lightly doped and fully depleted. This allows higher mobilities and hence higher performance. Moreover, since no doping is needed to confine the depletion region, discrete dopant number fluctuation is not a problem in FinFETs. Hence, the

threshold voltage is completely determined by the work function of the gate material.

Fabrication of FinFET devices is compatible with that of conventional MOS devices. This allows use of existing manufacturing facilities [8]. Reducing soft error rate and mitigating the impact of process variation in the circuits are becoming increasingly critical in CMOS technology where as in FinFET technology these difficulties are seen to be decreasing. FinFET is becoming a promising candidate, which exhibits excellent electrostatic control (i. e., suppression of SCE) and low voltage operability, thereby making it suitable for ultralow power operation [9].

Total power of the circuit is sum of leakage power and dynamic power. This research paper presents leakage power analysis of FinFET based and CMOS based inverter circuit. This analysis aids circuit designers who design circuits for battery-operated, portable and wearable applications [10]-[14].

This work is structured as follows. In section II, there is brief discussion about FinFET structure. In section III leakage power analysis is performed and other design metric analysis is also done. Conclusion is drawn in section IV.

## 2. FINFET STRUCTURE

The research community of University of California, Berkeley coined the term FinFET to describe a non-planar, double-gate transistor built on an SOI substrate [15]. FinFET technology has been born as a result of relentless increase in the levels of integration. It basically follows Moore's law which states that the number of transistors on a given area of silicon doubles every 2 years. Lower leakage current, superior performance and varied implementation styles are some of the reasons of popularity of FinFET. As per Moore's law scaling down offers high integration density on the chip and helps in the control of short channel effect. The low power consumption of FinFET allows high integration levels. FinFETs operate at a lower voltage as a result of their lower threshold voltage. The operating speed of FinFETs is 30% faster than non FinFET devices [16] [17]. The unique characteristic of the FinFET is that the conducting channel consists of thin silicon known as "fin", which forms the body of the device. FinFET is also known as non-planar double gate MOSFET (DG-MOSFET), in which both the front gate (FG) and back gate (BG) are tied together. A typical FinFET structure is shown in Fig. 1. Fin

width is negligibly smaller compared to Fin height ( $H_{fin}$ ). Larger device width can be realized by using multiple Fins. The scaling limit of FinFET is expressed in terms of  $\lambda$  as  $L_{min} \approx 1.5\lambda$ , where  $\lambda$  is given by  $W_{fin} + 2t_{ox}$ , where  $W_{fin}$  is silicon (fin) width and  $t_{ox}$  is insulator thickness. High-K gate dielectric material used in FinFET adds more advantage in terms of scaling, which can be easily achieved in FinFET. Oxide thickness ( $t_{ox}$ ) is limited by tunneling to  $\approx 2.5$  nm and fin width ( $W_{fin}$ ) is limited by threshold shift from quantum confinement to  $\approx 0.2$  nm. With these limiting values, the  $L_{min}$  (minimum channel length) of FinFET achievable is in the range from 5 to 10 nm [18]. The multiple electrically coupled gate and the thin silicon film layer helps in reducing the short channel effects (SCE).

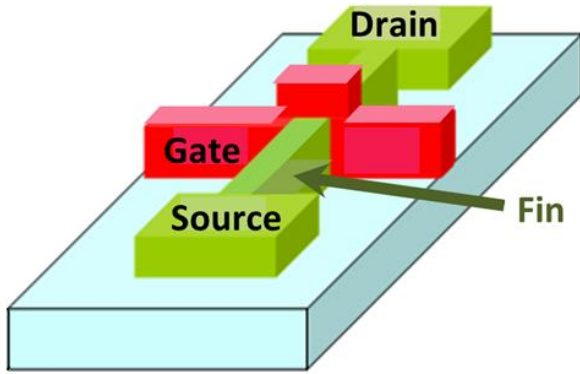


Fig 1: FINFET Structure.

### 3. APPLICATIONS OF FINFET BASED CIRCUITS

For applications like medical devices and sensor network nodes, using lower supply voltage can achieve lower energy consumption with acceptable speed. The minimum energy consumption is realized in sub-threshold region (where supply voltage is lower than the threshold voltage of device). In this region, off-state leakage can be utilized as the operating current to realize ultra-low power purpose [19]. In the past, conventional CMOS circuits were extensively studied for ultra-low power design and observed that leakage is prominent in these devices. Recently, research community described a non-planar device (FinFET) with ideal sub-threshold slope for sub-threshold operation due to its smaller gate capacitance and larger operating current for a given off-current. In FinFET devices leakage is observed to be lesser compared to conventional CMOS devices. FinFET is considered one of the most promising devices and this technology is applied in many other areas in semiconductor market [20]. One of the applications is in IoT (Internet of Things) technology.

Internet of Things (IoT) has unexpected growth potential but is split among many applications. One of the applications is wearable devices which consume ultra-low power. Wearable chip designing market is growing rapidly and the use of smarter things (IoT) by the consumers is driving the growth of the semiconductor industry mainly in the area of integrated circuit design. Because of this smart life, there became a necessity for the market to scale down the devices. The conventional MOSFET is reaching the scaling limits and the “end of technology road map”. Unfortunately Moore’s law is unable to continue. But the devices like FinFET are proving

its best to continue Moore’s law. FinFETs are implemented in IoT Technology to make the miniaturized world of things smarter and it seems to be the best option to choose FinFET device. Migration to smaller feature dimensions is major advantage for IoT. FinFET is highly competitive for Wi-Fi and Bluetooth combo chips that are used in IoT technology. For IoT, FinFET device provides ultra-low power consumption. FinFET is excellent technology for wide range of applications in IoT technology [21] [22].

### 4. RESULTS AND DISCUSSION

In this section leakage power analysis of FinFET based inverter and CMOS based inverter is done. Leakage power is the power consumed when the device is in off state. Leakage power reduction is very crucial in subthreshold circuits. In order to calculate leakage power of inverter, the input and output of the inverter are connected to two stage buffers as shown in Fig. 2. This set up is called as FO4 inverter chain. The circuit under test (CUT) is considered for the leakage power analysis. For this circuit under test, the input is considered as ‘c’ and output is considered as ‘d’. As the inverter is the nucleus of all digital designs and the electrical behavior of digital circuits can be almost totally derived by concluding the results obtained for inverter circuit [11], this work have taken inverter as a bench marking circuit for the analysis.

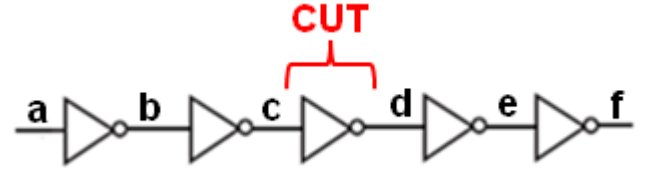


Fig 2: FO4 inverter chain simulated using 32-nm CMOS and FinFET predictive technology model parameters.

Leakage Power is mathematically expressed as

$$Leakage\ Power = I_{OFF} V_{DD}$$

Where  $I_{OFF}$  is leakage current and  $V_{DD}$  is supply voltage of the circuit. Subthreshold current in FinFET is expressed as

$$I_{DS} = \frac{q\mu_n V_T n_i^2}{N_a} \frac{e^{-\frac{V_s}{V_T}} - e^{-\frac{V_D}{V_T}}}{\int_0^{L_{eff}} \frac{dy}{\int_0^{H_{fin}} \int_0^{W_{fin}} e^{\frac{q\phi(x,y,z)}{KT}} dx dz}}$$

where  $N_a$  is the doping concentration of the Si-fin body,  $W_{fin}$ ,  $H_{fin}$ , and  $L_{eff}$  are the fin width, fin height, and channel length, respectively,  $V_D$  and  $V_S$  are the voltages for the drain and source terminals, respectively, and  $\phi$  is the potential distribution inside the fully depleted Si fin, which can be obtained by solving 3-D Poisson’s equation with adequate boundary conditions [23]. Leakage current is obtained when drain voltage is zero.

$$I_{OFF} = I_{DS} \text{ at } V_D = 0$$

In this paper, supply voltage is varied from 0.1 V to 0.45 V and leakage power of both CMOS based inverter and FinFET based inverter (circuit under test) are noted. Variability

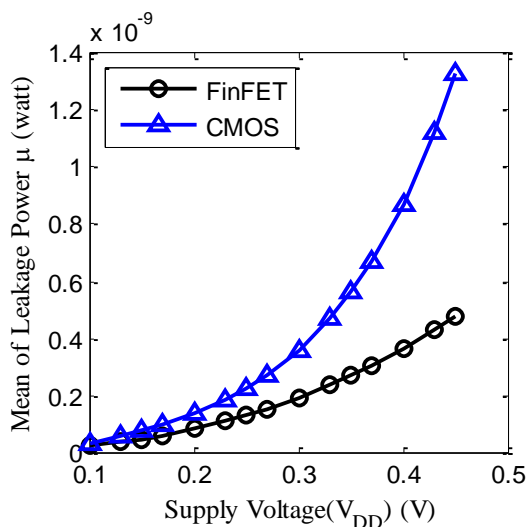
analysis of both is also performed and shown in Fig. 3. Variability is defined as the ratio of standard deviation to mean ( $\sigma/\mu$ ) of a design metric. It is observed that FinFET based inverter is less variable compared to that of CMOS based inverter. The leakage power in FinFET based inverter is very less compared to that of CMOS based inverter.

As the device shrinks, leakage increases. But it is found that a FinFET based circuit, at 32 nm technology node, with oxide thickness 0.9 nm, silicon film thickness 2 nm, dielectric constant of 3.9 and channel doping concentration of  $1 \times 10^{16} \text{ cm}^{-3}$  consumes lower leakage power as compared to that of CMOS based circuit. This work considers lightly doped channel region to avoid degrading of carrier mobility and threshold voltage variations. Short channel effects are also reduced. This makes the FinFET based circuit applicable for ultralow power operation. It is observed that there is  $1.58 \times (1.32 \times)$  improvements in mean value of leakage power (its variability). It is also seen in Fig. 3. In Fig. 4, it is imperative that power dissipation of FinFET based inverter is almost invariant, whereas power dissipation of CMOS based inverter varies with supply voltage variation. This implies that FinFET based devices and circuits are suitable for ultralow power applications like portable and wearable devices. In this paper, other design metrics like propagation delay (delay), power delay product (PDP) and energy delay product (EDP) at 0.1 V of supply voltage are observed and reported in Table I.

**Table I** Design metrics of FinFET based and CMOS based Inverter at supply voltage of 0.1 V

Inverter	Delay (sec)	PDP (w-s)	EDP (w-s <sup>2</sup> )
FinFET	1.276e-04	4.952e-15	9.514e-18
CMOS	1.281e-03	2.318e-14	4.861e-17

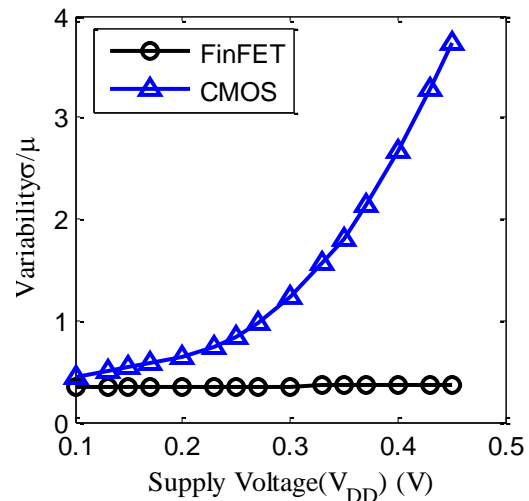
It is observed that FinFET based inverter exhibits desirable results in terms of delay, power-delay product and energy-delay product as compared to those of CMOS based inverter. FinFET based inverter achieves  $10.03 \times$  improvement in propagation delay. It means that FinFET based inverter is faster compared to CMOS based one. FinFET based inverter shows  $4.71 \times (5.11 \times)$  improvements in PDP (EDP) compared to CMOS based inverter.



**Fig 3:** Mean leakage power of FinFET based and CMOS based inverters versus supply voltage.

## 5. CONCLUSION

In this paper, leakage power and its variability analysis of FinFET and CMOS based inverters is performed. It is seen that the leakage power of FinFET based inverter is less variable compared to that of CMOS based inverter. As supply voltage varies the leakage power dissipation of CMOS inverter varies, whereas that of FinFET based inverter remains almost invariant. Moreover, FinFET based inverter is found to be faster (less propagation delay). It also consumes low leakage power compared to CMOS based inverter. Consequently, power-delay product and energy-delay product of FinFET based inverter are lower as compared to those of CMOS inverter. This work concludes by interpreting that FinFET based circuit is suitable for ultralow power applications like portable and wearable devices.



**Fig. 4 :** Variability of FinFET based and CMOS based inverters versus supply voltage.

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