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Elliptic Filter Implementation using Xilinx system Generator for Processing of ECG Signal

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ABSTRACT
Now a day's research has explore in development of prototype devices using different technology. The ECG processing is remained a important research topic as it is useful for the human being directly. Present paper deals with design and implementation of IIR Elliptic digital filter on FPGA for noise reduction in ECG Signal. In this paper filter designed with specifications like order 2, cutoff frequency 100Hz. The simulated results and complete step by step design of the filter is depicted in the paper. The results obtained shows the implementation is advantages considering area, power and Speed.

General Terms
Digital signal Processing, ECG, FPGA Technology.

Keywords
XSG, Elliptic Filter, noise Removal.

1. INTRODUCTION
Digital signal processing is promising field from last five decades [5,6]. Growth of DSP started in 1060's. This technology proved today for speed and optimal device utilization for prototype device development. Electrical activity of the heart is generally checked with the help of ECG Signal. ECG Signal provides important information of patient's heart condition. Many times while reading the ECG signal it gets corrupted because of different types of noise signal. Various methods are available for removing these noise contaminated in ECG signal. Many times the IIR and FIR digital filters are used to remove the noise from the ECG Signal There are different methods to remove the noise of the ECG signal which may include digital filters like IIR or FIR filter. Technological development has gifted FPGA technology and it has become more popular for rapid development of prototype devices. FPGA gives reduced board space and system power by reducing system power which leads to optimal device utilization. Field Programmable gate array (FPGA) chips operating speed is considerably large as compare to the DSP. There are top five benefits of the FPGA technology like Performance, Time to Market, Cost, Reliability, and Long-Term Maintenance. Now days this technique is used for implementation of digital filters. Different techniques are used by various researchers for implementation of IIR filter for different applications. In the implementation, representation of coefficients of filters is very important task. M.Z. Ikramet.al explained the method required for amplitude scaling and fixed point format representation [4]. Bahram Rashidi et.al have worked on reduction in power consumption of FIR filter using special adder and multipliers. They synthesized filter using Xilinx ISE Virtex IV FPGA and Xilinx Xpower analyzer [1]. Vladimir M. Poučki at.al have proposed sharpening technique for filter designing for higher order filter using similar low-order filters with same frequency specifications. As per their opinion this technique is used only for linear phase finite impulse response (FIR) filters. In their paper the method is applied on the elliptic IIR which have nonlinear phase. It is seen that transition width is significantly reduced by increase order of the filter. Filters have been implemented on FPGA and hardware folding technique [2]. Suva dip Roy at.al. Implemented a digital moving average filter on FPGA for noise reduction.[3]

This paper demonstrate the implementation of IIR filter using MATLAB Simulink model and Xilinx system generator blocks for high frequency noise reduction in ECG signal.

2. ELLIPTIC FILTER
An IIR filter of order M is generally demonstrated using difference equation,

$$y(n) + a_1 y(n-1) + a_2 y(n-2) + \cdots + a_N y(n-N) = b_0 x(n) + b_1 (n-1) + \ldots + b_M (n-M) \ldots\ldots 1$$

The Corresponding transfer function

$$H(z) = \frac{b_0 z^N + b_1 z^{N-1} + b_2 z^{N-2} + \cdots + b_M z^{N-M}}{z^N + a_1 z^{N-1} + a_2 z^{N-2} + \cdots + a_N} \ldots 2$$

These type of the filters are flexible than the FIR filter because of their feedback from previous output. As compared to FIR, denominator provides freedom in shape and response of the filter. Therefore design of IIR filter is simpler. These filters works on the approximations like Butterworth, Chebyshev and Elliptic. The Elliptic approximation has equiripple response in both passband and stopband. The frequency response magnitude of the elliptic filter of the order N is given by

$$\left|H_N(e^{j\omega})\right| = \left[\frac{1}{1+\varepsilon^2 G_N\left[tan(\omega/2)/tan(\omega_c/2)\right]^2}\right]^{1/2}$$

where $G_N(x)$ is a rational elliptic filter of the order N, ω_c is the cutoff frequency, and ε is a parameter which affects the passband ripples. It is possible to synthesize the this filter in matlab using code [B,A]elip(N,R_p, R_s, W_n,'ftype'). Similarly order of the filter can be calculated using code [N,Wn]=ellipord(Wp,Ws,Rp,Rs). This filter has unique property that they gives lowest filter order for given setoff specifications. If this filter is compared with FIR optimal filter which giving equiripple Frequency response. Therefore these filters are more preferred in IIR filters for various applications. These filters have some limitations that they have less linear phase in pass band as compare to Butterworth or chebyshev filter.

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3. DIGITAL FILTER INFORMATION

The digital filter information is given below in tabular form, the table 1 describes the detail information of Butterworth filter used for design, and whereas table 2 shows filter specifications used during implementation of filter, table 3 shows actual implementation cost in terms of number of components such as multipliers and adders used.

Table 1: Elliptic Filter Information

Filter structure	Direct form II
Number of sections	1
Filter Stability	Stable
Linear Phase	No
Design algorithm	Ellip

Table 2: Filter Design Specifications

Sampling frequency Fs	1000Hz
Filter response	Low pass
Filter order	2
Pass band edge	.2
3dB point	0.23963
6dB Point	0.28599
Stopband edge	0.97207
Pass band ripple	1db
Stop band attenuation	80 db
Transition width	0.77207

Table 3: Filter Implementation Cost

Number of Multipliers	4
Number of adders	4
Number of states	2
Multiplication per input sample	4
Addition per input sample	4

4. DESIGN SCHEME

To design elliptic filter for denoising ECG signal the filter order is taken 2 and the cut off frequency taken is 100 Hz. To get proper sampling and avoiding aliasing effect sampling frequency taken is 1000 Hz. Elliptic filter gives equiripple response in the pass and stop band.

4.1. Realization of Filter

The figure 1 shows design of Elliptic filter using FDA Tool whereas figure 2 shows realization model of the filter.

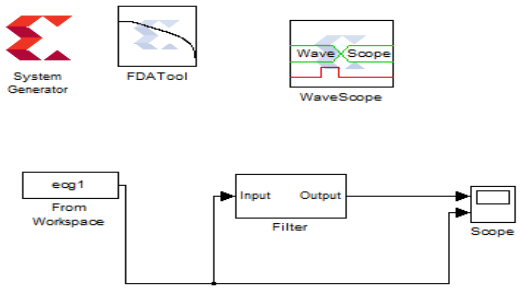

Fig.1: Design of IIR Elliptic filter using FDA tool

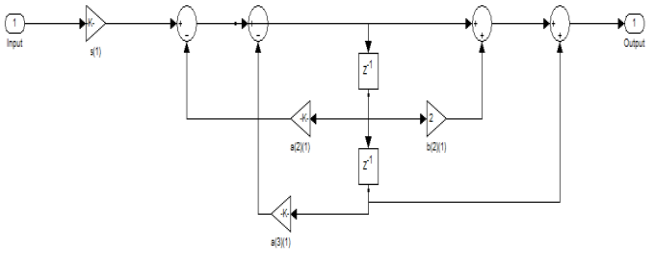

Fig.2: Realization model of IIR Elliptic Low pass filter using FDA Tool

4.2. Implementation Steps:

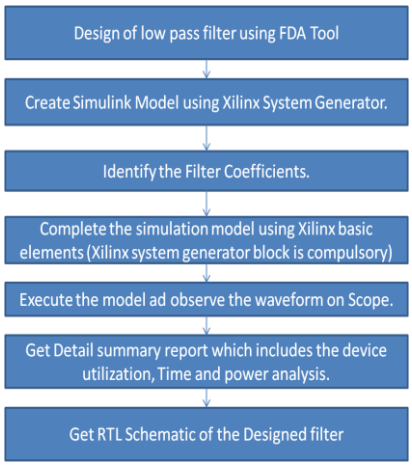

Fig.3: Implementation steps

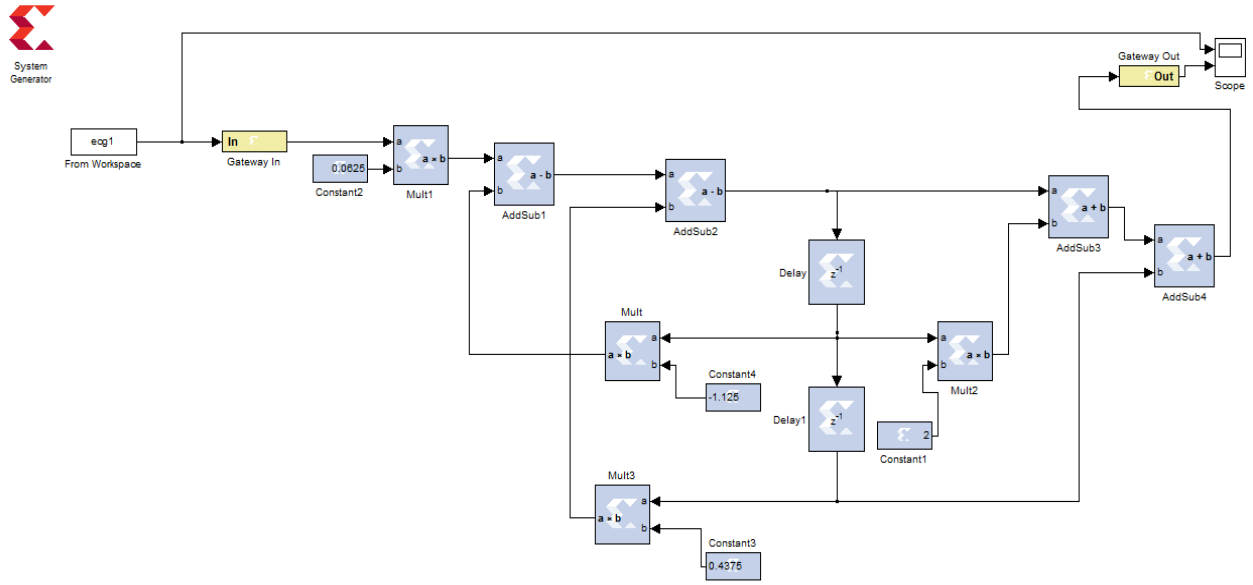

Fig.4 : IIR Elliptic Low pass filter using Xilinx System Generator

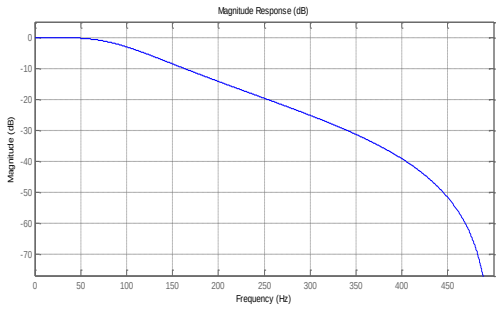

Fig.5a: Magnitude Response

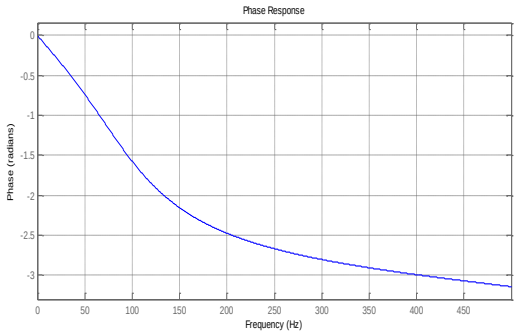

Fig.5b: Phase response

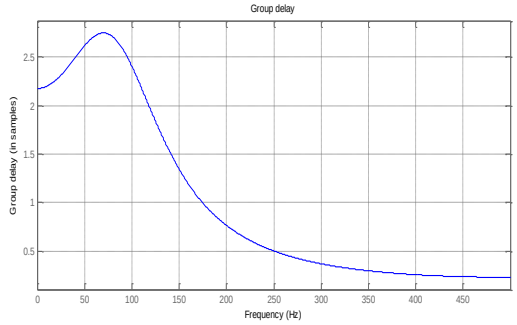

Fig.5c: Group Delay Response

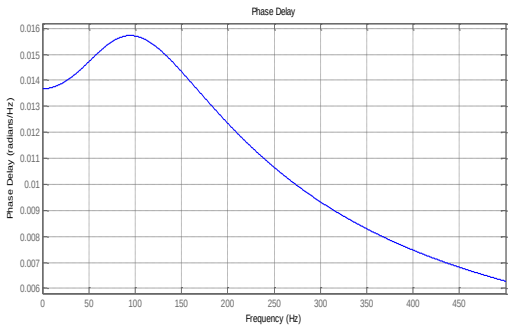

Fig.5d: Phase Delay Response

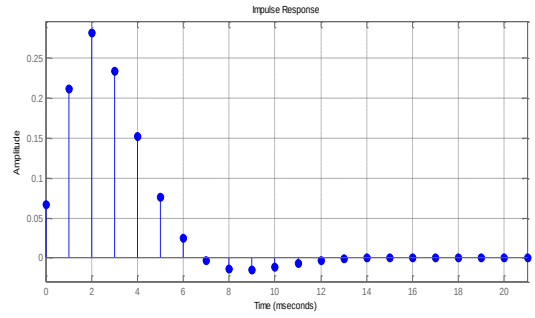

Fig.5e: Impulse Response

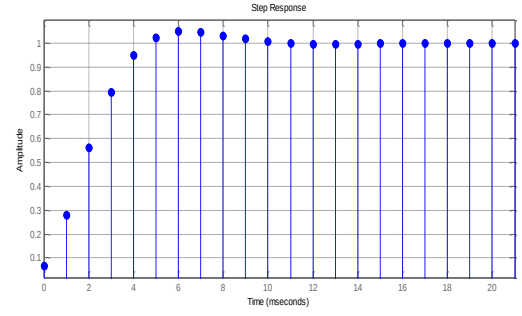

Fig.5f: Step Response

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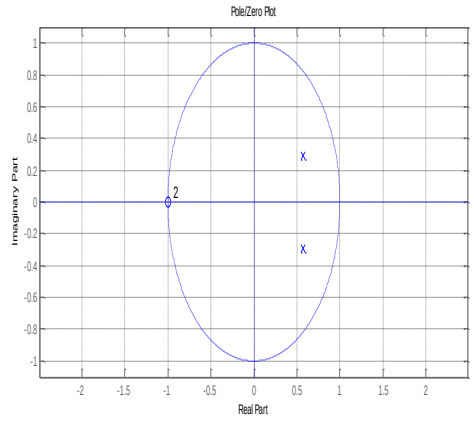

Fig.5g: Pole Zero Diagram

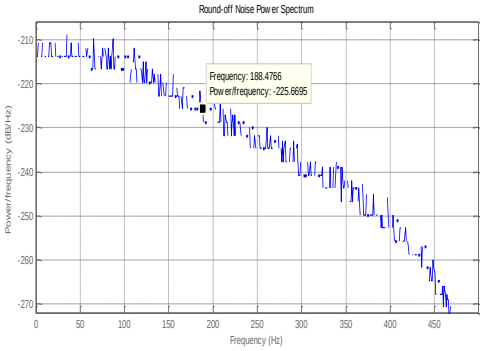

Fig.5h: Round off Noise power Spectrum

5. IMPLEMENTATION RESULTS

In this Filter ECG Signal is applied with High Freq Noise, The Figure 6 Shows Input & Output Waveforms before and after Filtration Where Noise above 100 Hz Is Filtered.

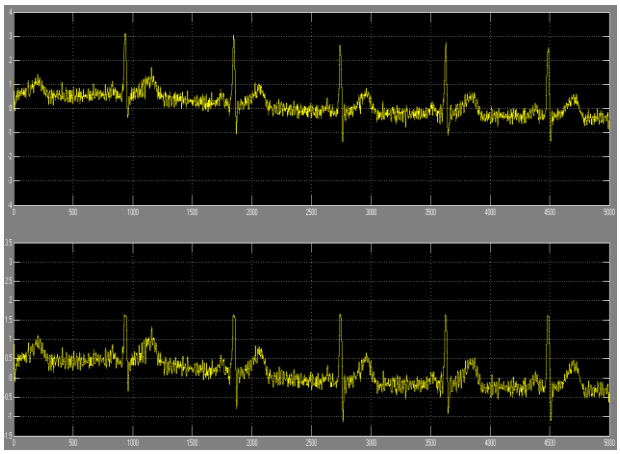

Fig.6: Input & Output waveforms of digital filter

5.1. RTL Schematic

Figure 7 shows the RTL Schematic of the proposed filter.

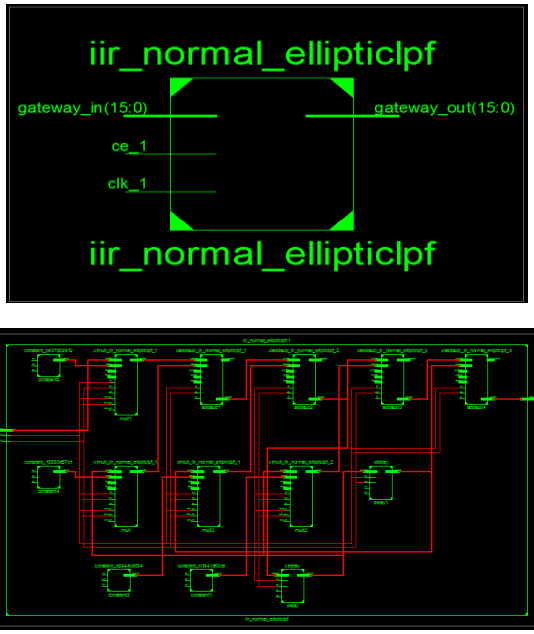

Fig.7: RTL Schematic

5.2. Device Utilization Summary

Target Device:	3s500efg320-4		
Product Version:	ISE 14.2		
Logic Utilization	**Available**	**Used**	**Utilization**
Number of Slice Flip Flops	9,312	4	1%
Number of 4 input LUTs	9,312	23	1%
Number of occupied Slices	4,656	40	1%
Number of Slices containing only related logic	40	40	100%
Number of Slices containing unrelated logic	40	0	0%
Total Number of 4 input LUTs	9,312	72	1%
Number used as logic		23	
Number used as a route-thru		49	
Number of bonded IOBs	232	33	14%
Number of BUFGMUXs	24	1	4%
Average Fanout of Non-Clock Nets		1.04	

6. CONCLUSION

In this paper low pass IIR Elliptic filter is designed and implemented for denoising the ECG signal using XSG Platform. It has been observed that filter shows good performance in terms of various parameters such as area, speed and power consumption. The filter implemented with Vedic multiplier can be used for various biomedical applications out of which one is used for denoising of ECG Signal. In future different order IIR and FIR filters can be implemented using Vedic multiplier for different applications.

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